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IN THE CLAIMS

Please amend the claims as follows.

1. (Previously Presented) A receive path circuit in a radio frequency (RF) receiver comprising:

a local oscillator (LO) circuit capable of (i) receiving a local oscillator (LO) reference signal having a frequency LO and a double sideband (DSB) clock signal having a frequency DSB and (ii) generating therefrom an in-phase product signal in which a polarity of said LO reference signal is reversed at said DSB frequency of said DSB clock signal; and

a first radio frequency (RF) mixer having a first input port capable of receiving said in-phase product signal and a second input port capable of receiving a modulated radio frequency (RF) signal, wherein said first RF mixer generating a first downconverted output signal.

2. (Previously Presented) The receive path circuit as set forth in Claim 1 wherein said LO circuit is further capable of generating a quadrature phase product signal ~~from~~ in which the polarity of said LO reference signal is reversed at said DSB frequency of said DSB clock signal.

3. (Previously Presented) The receive path circuit as set forth in Claim 2 further comprising a second radio frequency (RF) mixer having a first input port capable of receiving said quadrature phase product signal and a second input port capable of receiving said

modulated radio frequency (RF) signal, wherein said second RF mixer is capable of generating a second downconverted output signal.

4. (Previously Presented) The receive path circuit as set forth in Claim 3 wherein said LO circuit comprises a multiplier capable of receiving an in-phase LO reference signal and said DSB clock signal and generating therefrom said in-phase product signal.

5. (Original) The receive path circuit as set forth in Claim 4 wherein said multiplier is an analog multiplier.

6. (Original) The receive path circuit as set forth in Claim 4 wherein said multiplier is an exclusive-OR gate.

7. (Original) The receive path circuit as set forth in Claim 3 wherein said first downconverted output signal of said first RF mixer is a double-sideband suppressed carrier signal.

8. (Original) The receive path circuit as set forth in Claim 7 wherein said second downconverted output signal of said second RF mixer is a double-sideband suppressed carrier signal.

9. (Previously Presented) The receive path circuit as set forth in Claim 8 further comprising a first DSB filter block capable of receiving said first downconverted output signal and said DSB clock signal, wherein said first DSB filter block is capable of reversing a polarity of said first downconverted output signal at said DSB frequency of said DSB clock signal to thereby produce an in-phase baseband output signal.

10. (Previously Presented) The receive path circuit as set forth in Claim 9 further comprising a second DSB filter block capable of receiving said second downconverted output signal and said DSB clock signal, wherein said second DSB filter block is capable of reversing a polarity of said second downconverted output signal at said DSB frequency of said DSB clock signal to thereby produce a quadrature phase baseband output signal.

11. (Previously Presented) A radio frequency (RF) receiver comprising:

a receiver front-end circuit capable of receiving an incoming RF signal from an antenna and filtering and amplifying said incoming RF signal;

a local oscillator (LO) circuit capable of (i) receiving a local oscillator (LO) reference signal having a frequency LO and a double sideband (DSB) clock signal having a frequency DSB and (ii) generating therefrom an in-phase product signal in which a polarity of said LO reference signal is reversed at said DSB frequency of said DSB clock signal; and

a first radio frequency (RF) mixer having a first input port capable of receiving said in-phase product signal and a second input port capable of receiving said filtered and amplified incoming RF signal, wherein said first RF mixer is capable of generating a first downconverted output signal.

12. (Previously Presented) The radio frequency (RF) receiver as set forth in Claim 11 wherein said LO circuit is further capable of generating a quadrature phase product signal in which the polarity of said LO reference signal is reversed at said DSB frequency of said DSB clock signal.

13. (Previously Presented) The radio frequency (RF) receiver as set forth in Claim 12 further comprising a second radio frequency (RF) mixer having a first input port capable of receiving said quadrature phase product signal and a second input port capable of receiving said filtered and amplified incoming RF signal, wherein said second RF mixer is capable of generating a second downconverted output signal.

14. (Previously Presented) The radio frequency (RF) receiver as set forth in Claim 13 wherein said LO circuit comprises a multiplier capable of receiving an in-phase LO reference signal and said DSB clock signal and generating therefrom said in-phase product signal.

15. (Original) The radio frequency (RF) receiver as set forth in Claim 14 wherein said multiplier is an analog multiplier.

16. (Original) The radio frequency (RF) receiver as set forth in Claim 14 wherein said multiplier is an exclusive-OR gate.

17. (Original) The radio frequency (RF) receiver as set forth in Claim 13 wherein said first downconverted output signal of said first RF mixer is a double-sideband suppressed carrier signal.

18. (Original) The radio frequency (RF) receiver as set forth in Claim 17 wherein said second downconverted output signal of said second RF mixer is a double-sideband suppressed carrier signal.

19. (Previously Presented) The radio frequency (RF) receiver as set forth in Claim 18 further comprising a first DSB filter block capable of receiving said first downconverted output signal and said DSB clock signal, wherein said first DSB filter block is capable of reversing a polarity of said first downconverted output signal at said DSB frequency of said DSB clock signal to thereby produce an in-phase baseband output signal.

20. (Previously Presented) The radio frequency (RF) receiver as set forth in Claim 19 further comprising a second DSB filter block capable of receiving said second downconverted output signal and said DSB clock signal, wherein said second DSB filter block is capable of reversing a polarity of said second downconverted output signal at said DSB frequency of said DSB clock signal to thereby produce a quadrature phase baseband output signal.

21. (Previously Presented) A method, comprising:

receiving a local oscillator (LO) reference signal having a frequency LO and a double sideband (DSB) clock signal having a frequency DSB;

generating an in-phase product signal in which a polarity of the LO reference signal is reversed at the DSB frequency of the DSB clock signal; and

generating a downconverted output signal using the in-phase product signal and a modulated radio frequency (RF) signal.

22. (Previously Presented) The method of Claim 21, further comprising:

generating a quadrature phase product signal in which the polarity of the LO reference signal is reversed at the DSB frequency of the DSB clock signal; and

generating a second downconverted output signal using the quadrature phase product signal and the modulated RF signal.